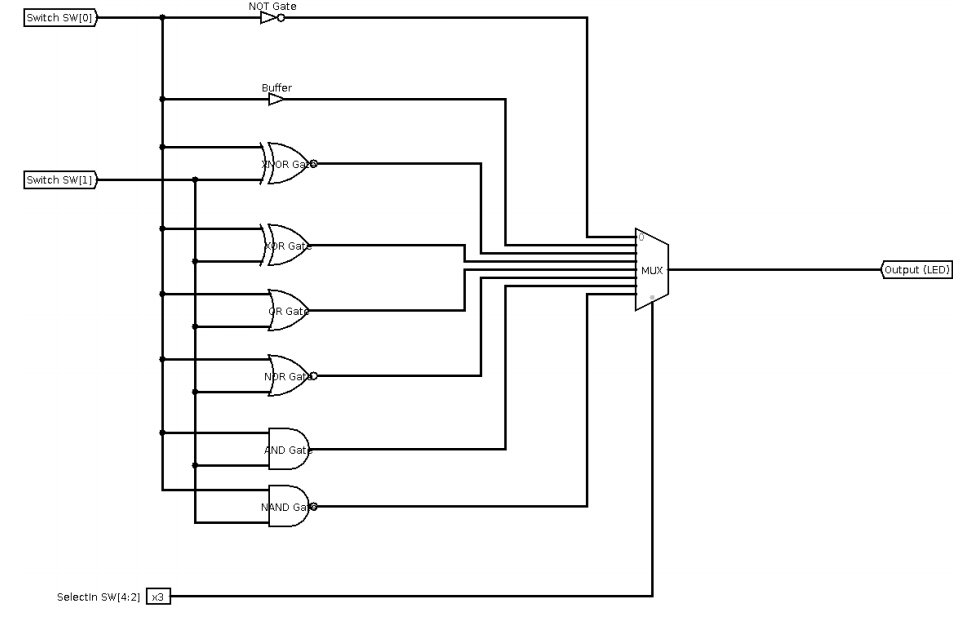
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EE M116L Lab Section 2

**Combinational Gates Muxed**



**2.** With this module, we used a multiplexer to choose from eight different combinational gate networks that had the output to an LED. We used switches as select bit inputs into the multiplexer and also used separate switches to provide input into the combinational gate networks that we chose.

**3.**

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\*.v

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module combinational\_gates\_muxed (led, sw);

// Input and output declaration

input [4:0] sw; // Inputs sw[7:5] are unused

output reg led; // Outputs led[7:1] are unused

// Declaring wires for the eight two inpuit basic gates

// Output Select Input Number

wire nand\_out; // 3'b111

wire and\_out; // 3'b110

wire nor\_out; // 3'b101

wire or\_out; // 3'b100

wire xor\_out; // 3'b011

wire xnor\_out; // 3'b010

wire buff\_out; // 3'b001

wire not\_out; // 3'b000

// 8-to-1 Multiplexer Inputs

wire [7:0] MuxIn;

wire [2:0] SelectIn;

// Generate outputs for the eight gates

assign nand\_out = ~(sw[0] & sw[1]); // 3'b111

assign and\_out = sw[0] & sw[1]; // 3'b110

assign nor\_out = ~(sw[0] | sw[1]); // 3'b101

assign or\_out = sw[0] | sw[1]; // 3'b100

assign xor\_out = sw[0] ^ sw[1]; // 3'b011

assign xnor\_out = sw[0] ^~ sw[1]; // 3'b010

assign buff\_out = sw[0]; // 3'b001

assign not\_out = ~sw[0]; // 3'b000

// 3'b111 3'b110 3'b101 3'b100 3'b011 3'b010 3'b001 3'b000

assign MuxIn = {nand\_out, and\_out, nor\_out, or\_out, xor\_out, xnor\_out, buff\_out, not\_out};

// Assigning select input lines for the multiplexer using switch lines SW7, SW6, and SW5

assign SelectIn = sw[4:2];

// Output multiplexer

always @(MuxIn, SelectIn)

led = MuxIn[SelectIn];

endmodule

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\*TB.v

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`timescale 1ns / 1ps

`include "combinational\_gates\_muxed.v" // Include the design description to be verified using testbench

module combinational\_gates\_muxed\_tb; // No inputs for a testbench!

// Inputs in the module to be tested will be port mapped to register variables

reg [4:0] sw\_T;

// Outputs in the module to be tested will be port mapped to wire variables

wire led\_T;

// Instantiation of the design module to be verified by the testbench

// Use named portmapping to map inputs to regsiter variables and outputs to

// wires

combinational\_gates\_muxed UUT (.sw(sw\_T),

.led(led\_T));

// Used for saving Value Change Dump (.vcd) file that records the waveforms of

// the simulation. Not needed while using Xilinx ISIM simulator.

initial

begin

$dumpfile("combinational\_gates\_muxed.vcd");

$dumpvars(2, combinational\_gates\_muxed\_tb.UUT);

end

// IMPORTANT: Initialize all inputs. Otherwise the default value of register

// will be don't care (x).

initial

begin

sw\_T = 5'h0;

end

// Use an always block to generate all the test cases

always

#5 sw\_T = sw\_T + 1'b1;

// Code to terminate simulation after all the test cases have been covered.

initial

#160 $finish; // After 160 timeunits, terminate simulation.

endmodule

===

\*.ucf

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## Leds

NET "led" LOC = "U16" | IOSTANDARD = "LVCMOS33"; #Bank = 2, Pin name = IO\_L2P\_CMPCLK, Sch name = LD0

## Switches

NET "sw<0>" LOC = "T10" | IOSTANDARD = "LVCMOS33"; #Bank = 2, Pin name = IO\_L29N\_GCLK2, Sch name = SW0

NET "sw<1>" LOC = "T9" | IOSTANDARD = "LVCMOS33"; #Bank = 2, Pin name = IO\_L32P\_GCLK29, Sch name = SW1

NET "sw<2>" LOC = "V9" | IOSTANDARD = "LVCMOS33"; #Bank = 2, Pin name = IO\_L32N\_GCLK28, Sch name = SW2

NET "sw<3>" LOC = "M8" | IOSTANDARD = "LVCMOS33"; #Bank = 2, Pin name = IO\_L40P, Sch name = SW3

NET "sw<4>" LOC = "N8" | IOSTANDARD = "LVCMOS33"; #Bank = 2, Pin name = IO\_L40N, Sch name = SW4

**4.**

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Advanced HDL Synthesis Report

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Macro Statistics

# Multiplexers : 1

1-bit 8-to-1 multiplexer : 1

# Xors : 2

1-bit xor2 : 2

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\* Design Summary \*

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Top Level Output File Name : combinational\_gates\_muxed.ngc

Primitive and Black Box Usage:

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# BELS : 1

# LUT5 : 1

# IO Buffers : 6

# IBUF : 5

# OBUF : 1

Device utilization summary:

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Selected Device : 6slx16csg324-3

Slice Logic Utilization:

Number of Slice LUTs: 1 out of 9112 0%

Number used as Logic: 1 out of 9112 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1

Number with an unused Flip Flop: 1 out of 1 100%

Number with an unused LUT: 0 out of 1 0%

Number of fully used LUT-FF pairs: 0 out of 1 0%

Number of unique control sets: 0

IO Utilization:

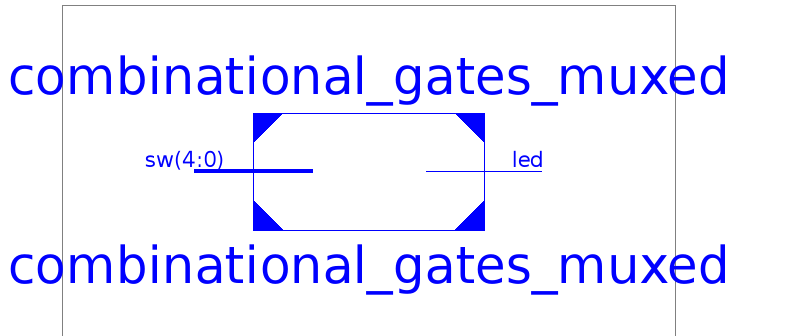
Number of IOs: 6

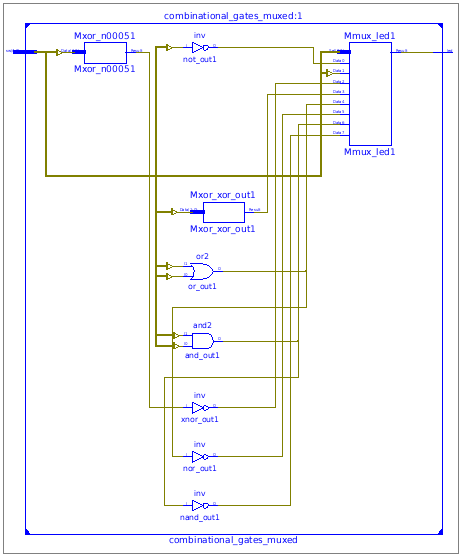
Number of bonded IOBs: 6 out of 232 2%

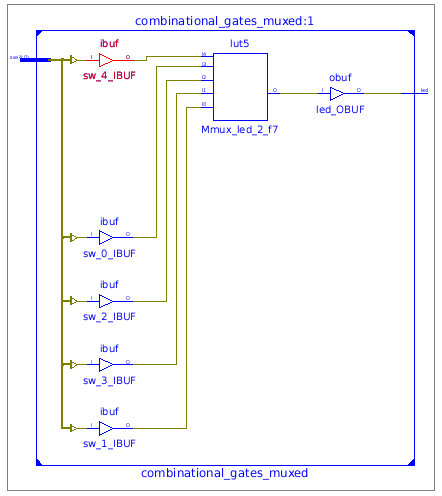
**5. Device Utilization Summary**

|  |  |  |  |
| --- | --- | --- | --- |
| Slice Logic Utilization | Used | Available | Utilization |
| # of Slice LUTs | 1 | 9,112 | 1% |
| #used at logic | 1 | 0,112 | 1% |
| #using O6 output only | 1 |  |  |
| # of occupied Slices | 1 | 2,278 | 1% |
| # of LUT Flip Flop pairs used | 1 |  |  |
| #with an unused Flip Flop | 1 | 1 | 100% |
| # of bonded IOBs | 6 | 232 | 2% |
| # of LOCed IOBs | 6 | 6 | 100% |
| Average Fanout of Non-Clock Nets | 1.00 |  |  |

**6. High Level Schematic**







**7. N/A**

**8. Waveform**

